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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of: **YONEDA, et al.**

Group Art Unit: **2814**

Serial No.: **09/442,038**

Examiner: **N. Ha**

Filed: **November 17, 1999**

P.T.O. Confirmation No.: 5343

For: **DEVICE HAVING RESIN PACKAGE AND METHOD OF PRODUCING THE SAME**

SUBMISSION OF APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, Va. 22313-1450

December 19, 2003

Sir:

Submitted herewith are an original and two copies of an Appeal Brief in the above-identified U.S. patent application.

Attached please find a check in the amount of $330.00 to cover the cost for the Appeal Brief.

If any additional fees are due in connection with this submission, please charge our Deposit Account No. 01-2340. This paper is filed in triplicate.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP

William L. Brooks
Attorney for Applicants
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PATENT TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF APPEALS

APPEAL BRIEF FOR THE APPELLANTS

Ex parte YONEDA et al.

DEVICE HAVING RESIN PACKAGE AND METHOD OF PRODUCING THE SAME

Serial Number: 09/442,038

Filed: November 17, 1999

Group Art Unit: 2814

Examiner: N. Ha

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Sir:

This is an appeal from the Office Action dated May 21, 2003 (Paper No. 26) in which claims 2, 5, 7-10, 15, 18, 20-22, 34-38 and 44-50 were finally rejected.

A Notice of Appeal and a Petition for Extension of Time were timely filed on October 21, 2003.

I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the subject application, which is:

Fujitsu Limited
1-1, Kamikodanaka 4-chome, Nakahara-ku
Kawasaki-shi, Kanagawa, JAPAN 211

II. RELATED APPEALS AND INTERFERENCES

Appellants know of no other appeals or interference proceedings related to the present appeal.

III. STATUS OF CLAIMS

Claims 2, 5, 7-10, 15, 18, 20-22, 34-38 and 44-50 on appeal have been finally rejected under 35 USC §103(a). Claims 27-33 and 39-41 are also pending but have been withdrawn from consideration and are not under appeal.

IV. STATUS OF AMENDMENTS

All amendments have been entered.

V. CLAIMS ON APPEAL

A clean copy of claims 2, 5, 7-10, 15, 18, 20-22, 34-38 and 44-50 on appeal is attached hereto as Exhibit A.

VI. SUMMARY OF THE INVENTION

The present invention generally relates to devices having a resin package, such as semiconductor devices, and more particularly to a resin-sealed semiconductor device of a leadless surface mounting type directed to high-density mounting. Further, the present invention is concerned with a method of producing such a semiconductor device.

The present invention comprises: a chip (111); a resin package (112, 151, 314) sealing the chip, the resin package having resin projections (117, 154, 318) located on a mount-side surface of the resin package; metallic films (113, 155, 315) respectively provided to the resin projections; and connecting parts (118, 101, 163, 245, 313, 341, 342) electrically connecting electrode pads of the chip and the metallic films. (Specification, page 35, lines 6-34; Figs. 32-34)

The device may be configured so that each of the metallic films is a single layer (113A) made of a metallic substance. (Specification, page 36, line 16 to page 38, line 16; Figs. 35-38)

The device may be configured so that: the connecting parts respectively comprise bonding wires (118), and bonding balls (101, 245) respectively provided to the metallic films; and the bonding wires are bonded to the electrode pads and the bonding balls. (Specification, page 35, lines 34-37)

The device may be configured so that the resin package (151) includes a first resin portion (153) on which the chip is provided, and a second resin portion (152) which covers the chip. (Specification, page 48, line 27 to page 49, line 23; Fig. 60)

The device may be configured so that: the connecting parts respectively comprise bonding wires (118), and connection electrodes (156) which are provided on the first resin portions and extend, into the resin projections, to the metallic films; and the bonding wires are bonded to the electrode pads and the connection electrodes. (Specification, page 49, lines 5-23)

The device may be configured so that the resin projections (154) respectively have through-holes (157) through which the connection electrodes extend to the metallic films. (Specification, page 49, line 7)

VII. THE ISSUES

1. Whether the invention, as recited in Appellants' claims 2, 5, 7-10, 15, 18, 20-22 and 34-36 on appeal, is unpatentable under 35 USC §103(a) over JP Application 63266374 to Hiroshi (hereinafter "**Hiroshi**") in view of JP 218509 to Atsushi (hereinafter "**Atsushi**") under 35 USC §103(a).

2. Whether the invention, as recited in Appellants' claims 37-38 and 44-50 on appeal, is unpatentable over **Hiroshi** and **Atsushi** in view of U.S. Patent 5,631,499 to Hosomi et al. (hereinafter "**Hosomi et al.**").

VIII. GROUPING OF THE CLAIMS

Rejected claims 2, 5, 7-10, 15, 18, 20-22, 34-38 and 44-50 rise and fall together because their patentability is argued collectively below.

IX. ARGUMENT WITH RESPECT TO THE ISSUES

A. THE REFERENCES

The Examiner has applied three prior art references to reject the claims, namely, **Hiroshi**, **Atsushi** and **Hosomi et al**.

1. **Hiroshi** discloses an integrated circuit device in which a through-hole 11a is provided through an insulating substrate 11, and a wiring board 10 is formed which includes a conductor exposed portion 12b on the opposite surface of an external

connection terminal surface 12a of a conductor 12a. Then, an integrated circuit element 13 is mounted on the wiring board 10 at a predetermined position of the same opposite to the conductor 12 of the insulating substrate 11 through a connection member 14 comprising insulative resin, and an adhesive material 14 is heated and hardened for adhesion and fixation of the insulated circuit element. Further, there is performed electrical connection required for an input/output electrode 13a of the integrated circuit elements 13a and the conductor exposed portion 12b of the wiring board 10. Thereafter the integrated circuit element 13, a metal wire 15, and the one surface of the insulating substrate 11 are covered with sealing resin 16 for protection thereof.

2. **Atsushi** discloses an optical semiconductor device in which connecting parts 6 projecting from the resin portion are completely covered by conductor pattern 2.

3. **Hosomi et al.** discloses a semiconductor device having a bump electrode including a first conductive layer formed on a predetermined portion of a substrate. An insulating layer is formed on the substrate and the first conductive layer. The insulating layer has an opening portion such that a predetermined portion of the first conductive layer is exposed. A second conductive layer is formed on the first conductive layer, a side wall of the opening portion of the insulating layer, and an upper surface of the insulating layer. A third conductive layer is formed to cover at least the insulating layer on the first conductive layer and the second conductive layer along the portion. A fourth conductive layer is formed on the third conductive layer

to have an over hang portion. A side etch portion is formed surrounded with an over hang portion of the fourth conductive layer, the third conductive layer, and the insulating layer.

B. SUMMARY OF EXAMINER'S REJECTIONS

In the Office Action of May 21, 2003, the Examiner rejected the claims as follows:

1. Claims 2, 5, 7-19, 15, 18, 20-22 and 34-36 were rejected under 35 USC §103(a) as unpatentable over **Hiroshi** in view of **Atsushi**.

In the Office Action, the Examiner urged that, in regard to claims 2, 7-10, 15, 20-22 and 34-36 on appeal, in Figs. 2-4, **Hiroshi** discloses a semiconductor device comprising:

a chip 13;

a resin package 16 sealing the chip, the resin package having resin projections located on a mount-side surface of the resin package, the projections projecting from a bottom surface of the device therein, as shown in Fig. 2, the chip being provided on the first resin portion 11 and covered by the second resin portion 16; and

connecting parts having bonding wire 15 and connection electrode 13a, where metallic films 12 are provided to the connection electrodes of the connecting parts.

Referring to Figure 7, the Examiner urged that the resin projection 38 has through-hole 34 through which the connection electrodes 33 extend to the metal film 32, as claimed in claim 9 on appeal.

The Examiner further urged that **Hiroshi** further discloses that the metallic film is provided on the bottom of the resin projections except the sides of the projections therein. The Examiner urged that **Atsushi** discloses an analogous semiconductor device including resin projections 6 and a metallic film that covering the projections on the bottom and the sides in order to make connections to the upper electrodes, as shown in Figs. 1-2.

The Examiner concluded that it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the metallic film, as taught by **Atsushi** in **Hiroshi** in order to make connections to the upper electrodes.

In regard to claim 10, the Examiner urged that **Hiroshi** further discloses the firs resin portion 11 comprising a resin tape 14, as shown in Fig. 2.

In regard to claim 34, the Examiner urged that **Atsushi** further discloses the metallic films are flush with the mount-side surface and exposed therefrom, as shown in Figs. 4b-5.

In regard to claims 35-36, the Examiner urged that their limitations are shown in Figs. 1-2 of **Atsushi**.

2. Claims 37-38 and 44-50 were rejected under 35 USC §103(a) as being unpatentable over **Hiroshi** and **Atsushi** as applied to claims 34-36 and further in view of **Hosomi et al**.

The Examiner urged that **Hiroshi**, as taught by **Atsushi**, discloses most aspects of the instant invention (paragraph 2) except for the metallic films comprising a plurality of metallic layer which

are stacked and the connecting parts comprising bumps provided between the electrode pads of the chip and the metallic films.

Referring to Fig. 11, the Examiner urged that **Hosomi et al.** teaches forming a metallic films 3 comprising a plurality of metallic layer which are stacked and the connecting parts comprising bump 6 provided between the electrode pads of the chip and the metallic films to improve intensity of adhesion between the bump electrode and the electrode pad (column 1, lines 29-30 and 32-33). The Examiner concluded that it would be obvious to one having ordinary skill in the art of the time the invention was made to form a bump between the electrode pads of the chip and metallic films as taught by **Hosomi et al.** in the device of **Hiroshi** to improve intensity of adhesion between the bump electrode and the electrode pad.

C. APPELLANTS' ARGUMENT

1. Claims 2, 5, 7-10, 15, 18, 20-22 and 34-36 on appeal are patentable over Hiroshi in view of Atsushi under 35 USC §103(a).

It is a basic tenet of patent law that to justify the use of a particular combination of prior art references to find a claim unpatentable, there must be a showing that the references themselves embody the specific claimed combination. This teaching was affirmed by the PTO U.S. Patent and Trademark Office Board of Patent Appeals and Interferences in *Ex parte Clapp*, 227 USPQ 972 (P.T.O. Bd. Pat. App. Int. 1985). This principle embodies the same concept propounded by the Court of Appeals for the Federal Circuit in that, not only must there be a teaching in the prior art of the structural elements of appellant's claimed invention, the prior art itself must actually suggest that

the structural elements be combined in a similar manner as the claimed invention. See, e.g., *Panduit Corp. v. Dennison Mfg. Co.*, 774 F.2d 1082, 227 USPQ 337 (Fed. Cir. 1985), **vacated on other grounds**, *Dennison Mfg. Co. v. Panduit Corp.*, 475 U.S. 809, 229 USPQ 478 (1986).

In Appellants' response of August 21, 2003, Applicants stated:

> It should be noted that conductor 12 in **Hiroshi**, corresponding to the metallic film of the present invention, covers only the bottom surface of the resin projection. This is in contrast to the present invention as shown, for example, in Fig. 32, in which the films 113 cover both the bottom and side surfaces of the resin projections.
>
> The Examiner has applied **Atsushi** for teaching this feature.
>
> Applicants respectfully disagree. Although **Atsushi** discloses an optical semiconductor device in which connecting parts 6 projecting from the resin portion are completely covered by conductor pattern 2, there would be no motivation to apply this teaching to **Hiroshi** because conductor 12 is a flat plate covering the bottom of sealing resin 16 and the wiring board 10. There is no "projection" in **Hiroshi**, only the flat plate. Thus, these references may not be combined to teach the present invention.

The Examiner now urges:

> In this case, the portion 1 of the Atsushi can be used to replace the bottom portion of the Hiroshi's device. This combination produces the structure that has conductive layer which covers the bottom and the sides of the projection portion as claimed. This combination is also proper since the connections to carry the signals from the chip are made through the conductor 2.

Appellants respectfully disagree. **Hiroshi** utilizes a plurality of flat conductor plates 12 to provide connection from the IC element 13 to the bottom of the package in view of the intended use of the device in a plastic IC card 21 as represented in Fig. 4 of **Hiroshi**. In contrast, **Atsushi** shows

four (4) projections 6 covered with a conductor pattern 2 arranged at each corner of the package, which connect the IC 3 to the bottom of the package. Thus, **Atsushi** utilizes projections for mounting while **Hiroshi** uses a plurality of flat plates for mounting. Thus, there would be no motivation for a person skilled in the art to form the projections taught by **Atsushi** on the flat bottom surface of the device of **Hiroshi**.

Furthermore, as noted in the response of August 21, 2003:

> Furthermore, with regard to claims 15 and 20-22, Applicants submit that the recited feature of "said resin projections extending downwards from the mount-surface and laterally extending from at least one of the resin package" is not disclosed in **Hiroshi**.

In the Office Action of May 21, 2003, the Examiner urged that:

> Hiroshi in fact discloses the resin profusion portions, where the bond wires 15 go through and connect to the bottom conductors. Furthermore, the resin 14 in Hiroshi is an adhesive material and can be considered as a resin tape. This resin layer performs the same function as the tape that disclosed in claim 34. The metallic layer 2 is flush with the surface as mentioned above; see also fig. 4b-5 of Atsushi.

The Examiner is incorrect and has apparently either disregarded or overlooked Appellants' argument that **Hiroshi** fails to teach the feature of resin projection projecting from the bottom surface of the device. What is disclosed in **Hiroshi** is a resin part projecting from the bottom surface of the chip, but this resin part of **Hiroshi** does not project from the bottom surface of the device. The device of **Hiroshi** has a flat bottom surface.

Furthermore, as stated in Applicants' August 21, 2003 response:

> In regard to claim 10, **Hiroshi** discloses that connection member 14 comprising "insulative" resin. Applicants submit that this material is not the same as "resin tape."

Thus, the 35 USC §103(a) rejection of claims 2, 5, 7-10, 15, 18, 20-22 and 34-36, on appeal, should be withdrawn.

2. Claims 37-38 and 44-50, on appeal, are patentable over the combination of Hiroshi, Atsushi and Hosomi et al. under 35 USC §103(a).

Hosomi et al. has been cited for teaching the formation of metallic films 3 comprising a plurality of stacked metallic layers but, like **Hiroshi** discussed above, fails to teach, mention or suggest the electrode forming a flush surface with the package body, as recited in claim 34, from which claims 37-38 depend.

Furthermore, none of the applied references teaches, mentions or suggests that metallic films are provided on the bottom and side surfaces of the resin projections, as recited in claims 44-50 on appeal.

In particular, it should be noted that **Hiroshi** has an insulating substrate 11 underneath the chip. Because the resin fills the gap formed in the insulating substrate 11, there appears apparent similarity, **if the insulating substrate 11 is removed**. However, the insulating substrate 11 forms a part of the device of **Hiroshi** and cannot be removed. Thus, the device of **Hiroshi** is characterized by a flat bottom surface, contrary to the device of the present invention.

With regard to **Atsushi**, it should be noted that the resin package body of **Atsushi** does have bottom projections, but the resin package body does not include the semiconductor chip therein.

Thus, **Atsushi** fails to teach the feature of the resin package **sealing the chip**, contrary to the present invention.

Thus, the 35 USC §103(a) rejection of claims 37-38 and 44-50 on appeal should be withdrawn.

X. CONCLUSION

For the above reasons, The Board of Patent Appeals and Interferences is therefore respectfully requested to reverse the Examiner's 35 USC §103(a) rejections of claims 2, 5, 7-10, 15, 18, 22-32, 34-38 and 44-50 on appeal and pass this application to issue.

In the event this paper is timely filed, Appellant hereby petitions for an appropriate extension of time. The fee for any such extension may be charged to Deposit Account No. 01-2340, along with any other additional fees which may be required with respect to this paper.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP

William L. Brooks
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Enclosure: Appendix A containing Claims on Appeal
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of: **YONEDA, et al.**

Group Art Unit: **2814**

Serial No.: **09/442,038**

Examiner: **N. Ha**

Filed: **November 17, 1999**

P.T.O. Confirmation No.: 5343

For: **DEVICE HAVING RESIN PACKAGE AND METHOD OF PRODUCING THE SAME**

CLAIMS ON APPEAL

Commissioner for Patents
P.O. Box 1450
Alexandria, Va 22313-1450

December 19, 2003

Sir:

The claims on appeal are 2, 5, 7-10, 15, 18, 20-22, 34-38 and 44-50, presented below.

Claim 2 (previously presented): A device comprising:

a chip;

a resin package sealing said chip, said resin package having resin projections located on a mount-side surface of the resin package, said projections projecting from a bottom surface of said device;

metallic films respectively provided to bottom and side surfaces of the resin projections; and

connecting parts electrically connecting electrode pads of said chip and the metallic films, wherein each of said metallic films is a single layer made of a metallic substance.

Claim 5 (previously presented): A device comprising:

a chip;

a resin package sealing said chip, said resin package having resin projections located on a mount-side surface of the resin package, said projections projecting from a bottom surface of said device;

metallic films respectively provided to bottom and side surfaces of the resin projections; and

connecting parts electrically connecting electrode pads of said chip and the metallic films, wherein:

said connecting parts respectively comprise bonding wires, and bonding balls respectively provided to the metallic films; and

said bonding wires are bonded to said electrode pads and said bonding balls.

Claim 7 (previously presented): A device comprising:

a chip;

a resin package sealing said chip, said resin package having resin projections located on a mount-side surface of the resin package, said projections projecting from a bottom surface of said device;

metallic films respectively provided to bottom and side surfaces of the resin projections; and

connecting parts electrically connecting electrode pads of said chip and the metallic films,

wherein said resin package includes a first resin portion on which the chip is provided, and a second resin portion which covers the chip.

Claim 8 (original): The device as claimed in claim 7, wherein: said connecting parts respectively comprise bonding wires, and connection electrodes which are provided on said first resin portions and extend, into the resin projections, to the metallic films; and said bonding wires are bonded to the electrode pads and the connection electrodes.

Claim 9 (original): The device as claimed in claim 8, wherein said resin projections respectively have through holes through which the connection electrodes extend to the metallic films.

Claim 10 (previously presented): A device comprising:

a chip;

a resin package sealing said chip and having a first resin portion and a second resin portion, said first resin portion comprising a resin tape and said chip being provided on said first resin portion and covered by said second resin portion;

connecting parts having bonding wires and connection electrodes, said connection electrodes being provided on the first resin portion and projecting therefrom; and

metallic films respectively provided to the connection electrodes of said connecting parts.

Claim 15 (previously presented): A device comprising:

a chip;

a resin package sealing said chip, said resin package having resin projections located on a mount-side surface of the resin package, said resin projections extending downwards from the mount-side surface and laterally extending from at least one side surface of the resin package;

metallic films respectively provided to bottom and side surfaces of the resin projections; and

connecting parts electrically connecting electrode pads of said chip and the metallic films,

wherein each of said metallic films is a single layer made of a metallic substance.

Claim 18 (previously presented): A device comprising:

a chip;

a resin package sealing said chip, said resin package having resin projections located on a mount-side surface of the resin package, said resin projections extending downwards from the mount-side surface and laterally extending from at least one side surface of the resin package;

metallic films respectively provided to bottom and side surfaces of the resin projections; and

connecting parts electrically connecting electrode pads of said chip and the metallic films,

wherein:

said connecting parts respectively comprise bonding wires, and bonding balls respectively provided to the metallic films; and

said bonding wires are bonded to said electrode pads and said bonding balls.

Claim 20 (previously presented): A device comprising:

a chip;

a resin package sealing said chip, said resin package having resin projections located on a mount-side surface of the resin package, said resin projections extending downwards from the mount-side surface and laterally extending from at least one side surface of the resin package;

metallic films respectively provided to bottom and side surfaces of the resin projections; and

connecting parts electrically connecting electrode pads of said chip and the metallic films,

wherein said resin projections laterally extend from a plurality of side surfaces of said resin package.

Claim 21 (previously presented): A device comprising:

a chip;

a resin package sealing said chip, said resin package having resin projections located on a mount-side surface of the resin package, said resin projections extending downwards from the mount-side surface and laterally extending from at least one side surface of the resin package;

metallic films respectively provided to bottom and side surfaces of the resin projections; and

connecting parts electrically connecting electrode pads of said chip and the metallic films,

wherein said resin projections laterally extend from only one side surface of said resin package.

Claim 22 (original): 22. The device as claimed in claim 20, further comprising supporting members provided to said resin package, said supporting members supporting the device vertically mounted on a circuit board.

Claim 34 (previously presented): A device comprising:

a chip;

a resin package sealing said chip, said resin package having a mount-side surface of the resin package which comprises a resin tape;

metallic films respectively provided in the resin package so that the metallic films are flush with the mount-side surface and are exposed therefrom; and

connecting parts electrically connecting electrode pads of said chip and the metallic films.

Claim 35 (original): The device as claimed in claim 34, wherein: said connecting parts respectively comprise bonding wires, and bonding balls respectively provided to the metallic films; and said bonding wires are bonded to said electrode pads and said bonding balls.

Claim 36 (original): The device as claimed in claim 34, wherein each of said metallic films is a single layer made of a metallic substance.

Claim 37 (original): The device as claimed in claim 34, wherein each of said metallic films comprises a plurality of metallic layers which are stacked.

Claim 38 (original): The device as claimed in claim 34, wherein said connecting parts respectively comprise bumps provided between the electrode pads of the chip and the metallic films.

Claim 44 (previously presented): A device comprising:

a chip;

a resin package sealing said chip, said resin package having resin projections located on a mount-side surface of the resin package, said projections projecting from a bottom surface of said device;

metallic films respectively provided to bottom and side surfaces of the resin projections; and

connecting parts electrically connecting electrode pads of said chip and the metallic films, wherein:

said connecting members respectively comprise bumps provided between the electrode pads of the chip and the metallic films.

Claim 45 (previously presented): A device comprising:

a chip;

a resin package sealing said chip, said resin package having resin projections located on a mount-side surface of the resin package, said projections projecting from a bottom surface of said device;

metallic films respectively provided to bottom and side surfaces of the resin projections; and

connecting parts electrically connecting electrode pads of said chip and the metallic films, wherein:

said metallic films respectively have lead portions, which are sealed by the resin package and extend toward the chip; and

said connecting parts include bumps provided between the electrode pads of the chip and the lead portions of the metallic films.

Claim 46 (previously presented): A device comprising:

a chip;

a resin package sealing said chip, said resin package having resin projections located on a mount-side surface of the resin package, said projections projecting from a bottom surface of said device;

metallic films respectively provided to bottom and side surfaces of the resin projections; and

connecting parts electrically connecting electrode pads of said chip and the metallic films, wherein:

said metallic films respectively have lead portions, which are sealed by the resin package and extend toward the chip, said lead portions having recess portions; and

said connecting parts include bumps, which are positioned in said recess portions and are provided between the electrodes pads of the chip and the lead portions of the metallic films.

Claim 47 (original): The device as claimed in claim 44, wherein a back surface of the chip opposite to a surface on which the electrode pads are provided is exposed from a surface of the resin package opposite to the mount-side surface thereof.

Claim 48 (original): The device as claimed in claim 47, further comprising a heat radiating member attached to the back surface of the chip.

Claim 49 (original): The device as claimed in claim 44, further comprising an insulating member provided to a surface of the chip on which the electrode pads are provided.

Claim 50 (original): The device as claimed in claim 44, wherein said connecting parts comprise an electrically conductive resin containing conductive particles joined together under a given pressure.

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Date: December 19, 2003
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A Notice of Appeal and a Petition for Extension of Time were timely filed on October 21, 2003.

I. REAL PARTY IN INTEREST

The real party in interest is the assignee of the subject application, which is:

Fujitsu Limited
1-1, Kamikodanaka 4-chome, Nakahara-ku
Kawasaki-shi, Kanagawa, JAPAN 211

II. RELATED APPEALS AND INTERFERENCES

Appellants know of no other appeals or interference proceedings related to the present appeal.

III. STATUS OF CLAIMS

Claims 2, 5, 7-10, 15, 18, 20-22, 34-38 and 44-50 on appeal have been finally rejected under 35 USC §103(a). Claims 27-33 and 39-41 are also pending but have been withdrawn from consideration and are not under appeal.

IV. STATUS OF AMENDMENTS

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VI. SUMMARY OF THE INVENTION

The present invention generally relates to devices having a resin package, such as semiconductor devices, and more particularly to a resin-sealed semiconductor device of a leadless surface mounting type directed to high-density mounting. Further, the present invention is concerned with a method of producing such a semiconductor device.

The present invention comprises: a chip (111); a resin package (112, 151, 314) sealing the chip, the resin package having resin projections (117, 154, 318) located on a mount-side surface of the resin package; metallic films (113, 155, 315) respectively provided to the resin projections; and connecting parts (118, 101, 163, 245, 313, 341, 342) electrically connecting electrode pads of the chip and the metallic films. (Specification, page 35, lines 6-34; Figs. 32-34)

The device may be configured so that each of the metallic films is a single layer (113A) made of a metallic substance. (Specification, page 36, line 16 to page 38, line 16; Figs. 35-38)

The device may be configured so that: the connecting parts respectively comprise bonding wires (118), and bonding balls (101, 245) respectively provided to the metallic films; and the bonding wires are bonded to the electrode pads and the bonding balls. (Specification, page 35, lines 34-37)

The device may be configured so that the resin package (151) includes a first resin portion (153) on which the chip is provided, and a second resin portion (152) which covers the chip. (Specification, page 48, line 27 to page 49, line 23; Fig. 60)

The device may be configured so that: the connecting parts respectively comprise bonding wires (118), and connection electrodes (156) which are provided on the first resin portions and extend, into the resin projections, to the metallic films; and the bonding wires are bonded to the electrode pads and the connection electrodes. (Specification, page 49, lines 5-23)

The device may be configured so that the resin projections (154) respectively have through-holes (157) through which the connection electrodes extend to the metallic films. (Specification, page 49, line 7)

VII. THE ISSUES

1. Whether the invention, as recited in Appellants' claims 2, 5, 7-10, 15, 18, 20-22 and 34-36 on appeal, is unpatentable under 35 USC §103(a) over JP Application 63266374 to Hiroshi (hereinafter "**Hiroshi**") in view of JP 218509 to Atsushi (hereinafter "**Atsushi**") under 35 USC §103(a).

2. Whether the invention, as recited in Appellants' claims 37-38 and 44-50 on appeal, is unpatentable over **Hiroshi** and **Atsushi** in view of U.S. Patent 5,631,499 to Hosomi et al. (hereinafter "**Hosomi et al.**").

VIII. GROUPING OF THE CLAIMS

Rejected claims 2, 5, 7-10, 15, 18, 20-22, 34-38 and 44-50 rise and fall together because their patentability is argued collectively below.

IX. ARGUMENT WITH RESPECT TO THE ISSUES

A. THE REFERENCES

The Examiner has applied three prior art references to reject the claims, namely, **Hiroshi**, **Atsushi** and **Hosomi et al**.

1. **Hiroshi** discloses an integrated circuit device in which a through-hole 11a is provided through an insulating substrate 11, and a wiring board 10 is formed which includes a conductor exposed portion 12b on the opposite surface of an external

connection terminal surface 12a of a conductor 12a. Then, an integrated circuit element 13 is mounted on the wiring board 10 at a predetermined position of the same opposite to the conductor 12 of the insulating substrate 11 through a connection member 14 comprising insulative resin, and an adhesive material 14 is heated and hardened for adhesion and fixation of the insulated circuit element. Further, there is performed electrical connection required for an input/output electrode 13a of the integrated circuit elements 13a and the conductor exposed portion 12b of the wiring board 10. Thereafter the integrated circuit element 13, a metal wire 15, and the one surface of the insulating substrate 11 are covered with sealing resin 16 for protection thereof.

2. **Atsushi** discloses an optical semiconductor device in which connecting parts 6 projecting from the resin portion are completely covered by conductor pattern 2.

3. **Hosomi et al.** discloses a semiconductor device having a bump electrode including a first conductive layer formed on a predetermined portion of a substrate. An insulating layer is formed on the substrate and the first conductive layer. The insulating layer has an opening portion such that a predetermined portion of the first conductive layer is exposed. A second conductive layer is formed on the first conductive layer, a side wall of the opening portion of the insulating layer, and an upper surface of the insulating layer. A third conductive layer is formed to cover at least the insulating layer on the first conductive layer and the second conductive layer along the portion. A fourth conductive layer is formed on the third conductive layer

to have an over hang portion. A side etch portion is formed surrounded with an over hang portion of the fourth conductive layer, the third conductive layer, and the insulating layer.

B. SUMMARY OF EXAMINER'S REJECTIONS

In the Office Action of May 21, 2003, the Examiner rejected the claims as follows:

1. Claims 2, 5, 7-19, 15, 18, 20-22 and 34-36 were rejected under 35 USC §103(a) as unpatentable over **Hiroshi** in view of **Atsushi**.

In the Office Action, the Examiner urged that, in regard to claims 2, 7-10, 15, 20-22 and 34-36 on appeal, in Figs. 2-4, **Hiroshi** discloses a semiconductor device comprising:

a chip 13;

a resin package 16 sealing the chip, the resin package having resin projections located on a mount-side surface of the resin package, the projections projecting from a bottom surface of the device therein, as shown in Fig. 2, the chip being provided on the first resin portion 11 and covered by the second resin portion 16; and

connecting parts having bonding wire 15 and connection electrode 13a, where metallic films 12 are provided to the connection electrodes of the connecting parts.

Referring to Figure 7, the Examiner urged that the resin projection 38 has through-hole 34 through which the connection electrodes 33 extend to the metal film 32, as claimed in claim 9 on appeal.

The Examiner further urged that **Hiroshi** further discloses that the metallic film is provided on the bottom of the resin projections except the sides of the projections therein. The Examiner urged that **Atsushi** discloses an analogous semiconductor device including resin projections 6 and a metallic film that covering the projections on the bottom and the sides in order to make connections to the upper electrodes, as shown in Figs. 1-2.

The Examiner concluded that it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the metallic film, as taught by **Atsushi** in **Hiroshi** in order to make connections to the upper electrodes.

In regard to claim 10, the Examiner urged that **Hiroshi** further discloses the firs resin portion 11 comprising a resin tape 14, as shown in Fig. 2.

In regard to claim 34, the Examiner urged that **Atsushi** further discloses the metallic films are flush with the mount-side surface and exposed therefrom, as shown in Figs. 4b-5.

In regard to claims 35-36, the Examiner urged that their limitations are shown in Figs. 1-2 of **Atsushi**.

2. Claims 37-38 and 44-50 were rejected under 35 USC §103(a) as being unpatentable over **Hiroshi** and **Atsushi** as applied to claims 34-36 and further in view of **Hosomi et al**.

The Examiner urged that **Hiroshi**, as taught by **Atsushi**, discloses most aspects of the instant invention (paragraph 2) except for the metallic films comprising a plurality of metallic layer which

are stacked and the connecting parts comprising bumps provided between the electrode pads of the chip and the metallic films.

Referring to Fig. 11, the Examiner urged that **Hosomi et al.** teaches forming a metallic films 3 comprising a plurality of metallic layer which are stacked and the connecting parts comprising bump 6 provided between the electrode pads of the chip and the metallic films to improve intensity of adhesion between the bump electrode and the electrode pad (column 1, lines 29-30 and 32-33). The Examiner concluded that it would be obvious to one having ordinary skill in the art of the time the invention was made to form a bump between the electrode pads of the chip and metallic films as taught by **Hosomi et al.** in the device of **Hiroshi** to improve intensity of adhesion between the bump electrode and the electrode pad.

C. APPELLANTS' ARGUMENT

1. Claims 2, 5, 7-10, 15, 18, 20-22 and 34-36 on appeal are patentable over Hiroshi in view of Atsushi under 35 USC §103(a).

It is a basic tenet of patent law that to justify the use of a particular combination of prior art references to find a claim unpatentable, there must be a showing that the references themselves embody the specific claimed combination. This teaching was affirmed by the PTO U.S. Patent and Trademark Office Board of Patent Appeals and Interferences in *Ex parte Clapp*, 227 USPQ 972 (P.T.O. Bd. Pat. App. Int. 1985). This principle embodies the same concept propounded by the Court of Appeals for the Federal Circuit in that, not only must there be a teaching in the prior art of the structural elements of appellant's claimed invention, the prior art itself must actually suggest that

the structural elements be combined in a similar manner as the claimed invention. See, e.g., *Panduit Corp. v. Dennison Mfg. Co.*, 774 F.2d 1082, 227 USPQ 337 (Fed. Cir. 1985), **vacated on other grounds**, *Dennison Mfg. Co. v. Panduit Corp.*, 475 U.S. 809, 229 USPQ 478 (1986).

In Appellants' response of August 21, 2003, Applicants stated:

> It should be noted that conductor 12 in **Hiroshi**, corresponding to the metallic film of the present invention, covers only the bottom surface of the resin projection. This is in contrast to the present invention as shown, for example, in Fig. 32, in which the films 113 cover both the bottom and side surfaces of the resin projections.
>
> The Examiner has applied **Atsushi** for teaching this feature.
>
> Applicants respectfully disagree. Although **Atsushi** discloses an optical semiconductor device in which connecting parts 6 projecting from the resin portion are completely covered by conductor pattern 2, there would be no motivation to apply this teaching to **Hiroshi** because conductor 12 is a flat plate covering the bottom of sealing resin 16 and the wiring board 10. There is no "projection" in **Hiroshi**, only the flat plate. Thus, these references may not be combined to teach the present invention.

The Examiner now urges:

> In this case, the portion 1 of the Atsushi can be used to replace the bottom portion of the Hiroshi's device. This combination produces the structure that has conductive layer which covers the bottom and the sides of the projection portion as claimed. This combination is also proper since the connections to carry the signals from the chip are made through the conductor 2.

Appellants respectfully disagree. **Hiroshi** utilizes a plurality of flat conductor plates 12 to provide connection from the IC element 13 to the bottom of the package in view of the intended use of the device in a plastic IC card 21 as represented in Fig. 4 of **Hiroshi**. In contrast, **Atsushi** shows

four (4) projections 6 covered with a conductor pattern 2 arranged at each corner of the package, which connect the IC 3 to the bottom of the package. Thus, **Atsushi** utilizes projections for mounting while **Hiroshi** uses a plurality of flat plates for mounting. Thus, there would be no motivation for a person skilled in the art to form the projections taught by **Atsushi** on the flat bottom surface of the device of **Hiroshi**.

Furthermore, as noted in the response of August 21, 2003:

> Furthermore, with regard to claims 15 and 20-22, Applicants submit that the recited feature of "said resin projections extending downwards from the mount-surface and laterally extending from at least one of the resin package" is not disclosed in **Hiroshi**.

In the Office Action of May 21, 2003, the Examiner urged that:

> Hiroshi in fact discloses the resin profusion portions, where the bond wires 15 go through and connect to the bottom conductors. Furthermore, the resin 14 in Hiroshi is an adhesive material and can be considered as a resin tape. This resin layer performs the same function as the tape that disclosed in claim 34. The metallic layer 2 is flush with the surface as mentioned above; see also fig. 4b-5 of Atsushi.

The Examiner is incorrect and has apparently either disregarded or overlooked Appellants' argument that **Hiroshi** fails to teach the feature of resin projection projecting from the bottom surface of the device. What is disclosed in **Hiroshi** is a resin part projecting from the bottom surface of the chip, but this resin part of **Hiroshi** does not project from the bottom surface of the device. The device of **Hiroshi** has a flat bottom surface.

Furthermore, as stated in Applicants' August 21, 2003 response:

> In regard to claim 10, **Hiroshi** discloses that connection member 14 comprising "insulative" resin. Applicants submit that this material is not the same as "resin tape."

Thus, the 35 USC §103(a) rejection of claims 2, 5, 7-10, 15, 18, 20-22 and 34-36, on appeal, should be withdrawn.

2. Claims 37-38 and 44-50, on appeal, are patentable over the combination of Hiroshi, Atsushi and Hosomi et al. under 35 USC §103(a).

Hosomi et al. has been cited for teaching the formation of metallic films 3 comprising a plurality of stacked metallic layers but, like **Hiroshi** discussed above, fails to teach, mention or suggest the electrode forming a flush surface with the package body, as recited in claim 34, from which claims 37-38 depend.

Furthermore, none of the applied references teaches, mentions or suggests that metallic films are provided on the bottom and side surfaces of the resin projections, as recited in claims 44-50 on appeal.

In particular, it should be noted that **Hiroshi** has an insulating substrate 11 underneath the chip. Because the resin fills the gap formed in the insulating substrate 11, there appears apparent similarity, **if the insulating substrate 11 is removed**. However, the insulating substrate 11 forms a part of the device of **Hiroshi** and cannot be removed. Thus, the device of **Hiroshi** is characterized by a flat bottom surface, contrary to the device of the present invention.

With regard to **Atsushi**, it should be noted that the resin package body of **Atsushi** does have bottom projections, but the resin package body does not include the semiconductor chip therein.

Thus, **Atsushi** fails to teach the feature of the resin package **sealing the chip**, contrary to the present invention.

Thus, the 35 USC §103(a) rejection of claims 37-38 and 44-50 on appeal should be withdrawn.

X. CONCLUSION

For the above reasons, The Board of Patent Appeals and Interferences is therefore respectfully requested to reverse the Examiner's 35 USC §103(a) rejections of claims 2, 5, 7-10, 15, 18, 22-32, 34-38 and 44-50 on appeal and pass this application to issue.

In the event this paper is timely filed, Appellant hereby petitions for an appropriate extension of time. The fee for any such extension may be charged to Deposit Account No. 01-2340, along with any other additional fees which may be required with respect to this paper.

Respectfully submitted,

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Enclosure: Appendix A containing Claims on Appeal
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of: **YONEDA, et al.**

Group Art Unit: **2814**

Serial No.: **09/442,038**

Examiner: **N. Ha**

Filed: **November 17, 1999**

P.T.O. Confirmation No.: 5343

For: **DEVICE HAVING RESIN PACKAGE AND METHOD OF PRODUCING THE SAME**

CLAIMS ON APPEAL

Commissioner for Patents
P.O. Box 1450
Alexandria, Va 22313-1450

December 19, 2003

Sir:

The claims on appeal are 2, 5, 7-10, 15, 18, 20-22, 34-38 and 44-50, presented below.

Claim 2 (previously presented): A device comprising:

a chip;

a resin package sealing said chip, said resin package having resin projections located on a mount-side surface of the resin package, said projections projecting from a bottom surface of said device;

metallic films respectively provided to bottom and side surfaces of the resin projections; and

connecting parts electrically connecting electrode pads of said chip and the metallic films, wherein each of said metallic films is a single layer made of a metallic substance.

Claim 5 (previously presented): A device comprising:

a chip;

a resin package sealing said chip, said resin package having resin projections located on a mount-side surface of the resin package, said projections projecting from a bottom surface of said device;

metallic films respectively provided to bottom and side surfaces of the resin projections; and

connecting parts electrically connecting electrode pads of said chip and the metallic films, wherein:

said connecting parts respectively comprise bonding wires, and bonding balls respectively provided to the metallic films; and

said bonding wires are bonded to said electrode pads and said bonding balls.

Claim 7 (previously presented): A device comprising:

a chip;

a resin package sealing said chip, said resin package having resin projections located on a mount-side surface of the resin package, said projections projecting from a bottom surface of said device;

metallic films respectively provided to bottom and side surfaces of the resin projections; and

connecting parts electrically connecting electrode pads of said chip and the metallic films,

wherein said resin package includes a first resin portion on which the chip is provided, and a second resin portion which covers the chip.

Claim 8 (original): The device as claimed in claim 7, wherein: said connecting parts respectively comprise bonding wires, and connection electrodes which are provided on said first resin portions and extend, into the resin projections, to the metallic films; and said bonding wires are bonded to the electrode pads and the connection electrodes.

Claim 9 (original): The device as claimed in claim 8, wherein said resin projections respectively have through holes through which the connection electrodes extend to the metallic films.

Claim 10 (previously presented): A device comprising:

a chip;

a resin package sealing said chip and having a first resin portion and a second resin portion, said first resin portion comprising a resin tape and said chip being provided on said first resin portion and covered by said second resin portion;

connecting parts having bonding wires and connection electrodes, said connection electrodes being provided on the first resin portion and projecting therefrom; and

metallic films respectively provided to the connection electrodes of said connecting parts.

Claim 15 (previously presented): A device comprising:

a chip;

a resin package sealing said chip, said resin package having resin projections located on a mount-side surface of the resin package, said resin projections extending downwards from the mount-side surface and laterally extending from at least one side surface of the resin package;

metallic films respectively provided to bottom and side surfaces of the resin projections; and

connecting parts electrically connecting electrode pads of said chip and the metallic films,

wherein each of said metallic films is a single layer made of a metallic substance.

Claim 18 (previously presented): A device comprising:

a chip;

a resin package sealing said chip, said resin package having resin projections located on a mount-side surface of the resin package, said resin projections extending downwards from the mount-side surface and laterally extending from at least one side surface of the resin package;

metallic films respectively provided to bottom and side surfaces of the resin projections; and

connecting parts electrically connecting electrode pads of said chip and the metallic films,

wherein:

said connecting parts respectively comprise bonding wires, and bonding balls respectively provided to the metallic films; and

said bonding wires are bonded to said electrode pads and said bonding balls.

Claim 20 (previously presented): A device comprising:

a chip;

a resin package sealing said chip, said resin package having resin projections located on a mount-side surface of the resin package, said resin projections extending downwards from the mount-side surface and laterally extending from at least one side surface of the resin package;

metallic films respectively provided to bottom and side surfaces of the resin projections; and

connecting parts electrically connecting electrode pads of said chip and the metallic films,

wherein said resin projections laterally extend from a plurality of side surfaces of said resin package.

Claim 21 (previously presented): A device comprising:

a chip;

a resin package sealing said chip, said resin package having resin projections located on a mount-side surface of the resin package, said resin projections extending downwards from the mount-side surface and laterally extending from at least one side surface of the resin package;

metallic films respectively provided to bottom and side surfaces of the resin projections; and

connecting parts electrically connecting electrode pads of said chip and the metallic films,

wherein said resin projections laterally extend from only one side surface of said resin package.

Claim 22 (original): 22. The device as claimed in claim 20, further comprising supporting members provided to said resin package, said supporting members supporting the device vertically mounted on a circuit board.

Claim 34 (previously presented): A device comprising:

a chip;

a resin package sealing said chip, said resin package having a mount-side surface of the resin package which comprises a resin tape;

metallic films respectively provided in the resin package so that the metallic films are flush with the mount-side surface and are exposed therefrom; and

connecting parts electrically connecting electrode pads of said chip and the metallic films.

Claim 35 (original): The device as claimed in claim 34, wherein: said connecting parts respectively comprise bonding wires, and bonding balls respectively provided to the metallic films; and said bonding wires are bonded to said electrode pads and said bonding balls.

Claim 36 (original): The device as claimed in claim 34, wherein each of said metallic films is a single layer made of a metallic substance.

Claim 37 (original): The device as claimed in claim 34, wherein each of said metallic films comprises a plurality of metallic layers which are stacked.

Claim 38 (original): The device as claimed in claim 34, wherein said connecting parts respectively comprise bumps provided between the electrode pads of the chip and the metallic films.

Claim 44 (previously presented): A device comprising:

a chip;

a resin package sealing said chip, said resin package having resin projections located on a mount-side surface of the resin package, said projections projecting from a bottom surface of said device;

metallic films respectively provided to bottom and side surfaces of the resin projections; and

connecting parts electrically connecting electrode pads of said chip and the metallic films, wherein:

said connecting members respectively comprise bumps provided between the electrode pads of the chip and the metallic films.

Claim 45 (previously presented): A device comprising:

a chip;

a resin package sealing said chip, said resin package having resin projections located on a mount-side surface of the resin package, said projections projecting from a bottom surface of said device;

metallic films respectively provided to bottom and side surfaces of the resin projections; and

connecting parts electrically connecting electrode pads of said chip and the metallic films, wherein:

said metallic films respectively have lead portions, which are sealed by the resin package and extend toward the chip; and

said connecting parts include bumps provided between the electrode pads of the chip and the lead portions of the metallic films.

Claim 46 (previously presented): A device comprising:

a chip;

a resin package sealing said chip, said resin package having resin projections located on a mount-side surface of the resin package, said projections projecting from a bottom surface of said device;

metallic films respectively provided to bottom and side surfaces of the resin projections; and

connecting parts electrically connecting electrode pads of said chip and the metallic films, wherein:

said metallic films respectively have lead portions, which are sealed by the resin package and extend toward the chip, said lead portions having recess portions; and

said connecting parts include bumps, which are positioned in said recess portions and are provided between the electrodes pads of the chip and the lead portions of the metallic films.

Claim 47 (original): The device as claimed in claim 44, wherein a back surface of the chip opposite to a surface on which the electrode pads are provided is exposed from a surface of the resin package opposite to the mount-side surface thereof.

Claim 48 (original): The device as claimed in claim 47, further comprising a heat radiating member attached to the back surface of the chip.

Claim 49 (original): The device as claimed in claim 44, further comprising an insulating member provided to a surface of the chip on which the electrode pads are provided.

Claim 50 (original): The device as claimed in claim 44, wherein said connecting parts comprise an electrically conductive resin containing conductive particles joined together under a given pressure.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF APPEALS

APPEAL BRIEF FOR THE APPELLANTS

Ex parte YONEDA et al.

DEVICE HAVING RESIN PACKAGE AND METHOD OF PRODUCING THE SAME

Serial Number: 09/442,038

Filed: November 17, 1999

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Examiner: N. Ha

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